DETAILED ACTION

1. The amendment filed 06/18/07 has being acknowledged and entered. By this amendment claims 1-13 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 6-7 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007).

Regarding claim 1, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3pd/3nd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region (3nd/3pd); a second wiring layer 13L formed on said semiconductor substrate 1 above said first wiring layer 21C; and a bonding pad 102 to be electrically connected to an external connection terminal, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least a part of said bonding pad 102 being located above said operating region (3nd/3pd), wherein said second wiring layer 13L includes a plurality of

wirings formed in the region under said bonding pad 102, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316; said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20).

The embodiment shown in Fig. 60 of Saito does not teach that the at least one of the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer.

However, another embodiment shown in Fig. 1 of Saito teaches that the at least one of the other wiring 13L (on right side) of the second wiring layer 13L is electrically connected to both the first wiring layer 12C (on right side) and the operation region 3pd by way of the first wiring layer 12C in order to provide electrical connection to the

component form in the substrate. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the device of the embodiment shown in Fig. 60 of Saito by forming the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer in order to provide electrical connection to the component form in the substrate, as taught by another embodiment shown in Fig. 1 of Saito.

Regarding claim 6, Saito (Fig. 60) discloses the semiconductor device wherein the bonding pad 102 is to be electrically connected to an inner lead by an inner lead bonding process. The bonding pad of Saito is capable of electrically connected "to an inner lead by an inner lead. It is note that the process limitation "by an inner lead bonding process" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). In addition "to be electrically connected to an inner lead" does not define any distinct structure.

Regarding claim 7, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3nd/3pd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region (3nd/3pd); a second wiring layer 13L formed on said semiconductor substrate 1 above said first

wiring layer 21C; and a bonding pad 102 to be electrically connected to an inner lead, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least a part of said bonding pad 102 being located above said operating region (3nd/3pd), wherein said second wiring layer 13L includes a plurality of wirings formed in the region under said bonding pad 102, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316; said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges of the regions electrically connected to the inner lead on the surface of the bonding pad 102 (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20). It is note that the process limitation "by an inner lead bonding process" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964

(Fed. Cir. 1985). In addition "to be electrically connected to an inner lead" does not define any distinct structure.

The embodiment shown in Fig. 60 of Saito does not teach that the at least one of the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer.

However, another embodiment shown in Fig. 1 of Saito teaches that the at least one of the other wiring 13L (on right side) of the second wiring layer 13L is electrically connected to both the first wiring layer 12C (on right side) and the operation region 3pd by way of the first wiring layer 12C in order to provide electrical connection to the component form in the substrate. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the device of the embodiment shown in Fig. 60 of Saito by forming the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer in order to provide electrical connection to the component form in the substrate, as taught by another embodiment shown in Fig. 1 of Saito.

Regarding claim 10, Saito discloses the semiconductor device wherein said insulating film 15 is made up of a silicone oxide film and a silicone nitride film (col. 18, lines 14-20). It is note that the process limitation "formed by CVD" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 11, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3nd/3pd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region (3nd/3pd); a second wiring layer 13L formed on said semiconductor substrate 1 above said first wiring layer 21C; and a bonding pad 102 to be electrically connected to an external connection terminal, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least a part of said bonding pad 102 being located above said operating region (3nd/3pd), wherein said second wiring layer 13L includes a plurality of wirings, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316; said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said

insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20).

Saito does not expressly disclose under the edges in the lengthwise direction of bonding pad to 3 micron outside the region. It would have been obvious to one of ordinary skill in art to use the general distance teaching of Saito in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233,235 (CCPA 1955). In this case, there is nothing in the present application to indicate that the claimed under the edges in the lengthwise direction of bonding pad to 3 micron outside the region is critical. Therefore, the forming under the edges in the lengthwise direction of bonding pad to 3 micron outside the region can be optimized during experimentation depending upon operating the device in a particular application.

The embodiment shown in Fig. 60 of Saito does not teach that the at least one of the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer.

However, another embodiment shown in Fig. 1 of Saito teaches that the at least one of the other wiring 13L (on right side) of the second wiring layer 13L is electrically connected to both the first wiring layer 12C (on right side) and the operation region 3pd by way of the first wiring layer 12C in order to provide electrical connection to the component form in the substrate. Accordingly, it would have been obvious to one of

ordinary skill in the art at the time of the invention was made to modify the device of the embodiment shown in Fig. 60 of Saito by forming the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer in order to provide electrical connection to the component form in the substrate, as taught by another embodiment shown in Fig. 1 of Saito.

Regarding claim 12, Saito discloses the semiconductor device wherein said insulating film 15 is made up of an inorganic insulating film only.

Regarding claim 13, Saito discloses the semiconductor device wherein at least a part of said other wirings 13L is formed in a region right under said bonding pad 102, and other wirings formed in the region right under the bonding pad 102 are formed only in a region right under a region electrically connected to an inner lead on a surface of said bonding pad 102 (Fig. 60).

4. Claims 2-5 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007) in view of Applicant Admitted Prior Art (APA).

Regarding claims 2-3, 8-9, Saito does not discloses the in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 micron to 3 micron.

However, APA discloses (Fig. 9) a semiconductor device comprises a wire 202 having bonding pad 201, an expanded regions right under said expanded regions 201a-b as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal 208, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad 201 are set to fall in a range of from 2 micron (see background of the invention in fig. 9). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to conclude that the bonding pad 102 of Saito would have the expanded regions as claimed. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 195 USPQ 430,433 (CCPA 1977).

Regarding claims 4-5, Saito does not disclose the semiconductor device wherein said bonding pad 102 and said external connection terminal are electrically connected by the chip-on-glass or chip-on board.

However, APA discloses the semiconductor device wherein bonding pad 201 and said external connection terminal are electrically connected by the chip-on-glass (COG) or TCP (see background of the invention). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the teaching of APA with Saito for intended use because the recitation "chip-on-glass" or "chip-on-board" of the claimed invention does not result in a structural difference between the

claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Response to Arguments

5. Applicant's arguments filed on 06/18/07 have been fully considered but are moot in view of the new ground(s) of rejection.

6. Applicant argues that "in Fig. 60 of Saito the right-most wiring 13L of the second wiring layer which is insulated from the alleged bonding pad 102 via insulator 15 is not electrically connected to the alleged operating region 3nd".

The examiner agreed that the embodiment shown in Fig. 60 of Saito does not teach that the at least one of the other wiring of the second wiring layer is electrically connected to both the first wiring layer and the operation region by way of the first wiring layer. However, another embodiment shown in Fig. 1 of Saito teaches that the at least one of the other wiring 13L (on right side) of the second wiring layer 13L is electrically connected to both the first wiring layer 12C (on right side) and the operation region 3pd by way of the first wiring layer 12C.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday, Tuesday and Thursday from 7:00AM - 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Theresa T. Doan/
Primary Examiner, Art Unit 2814